Characterization of ESD Risks in an Assembly Process by Using Component-Level CDM Withstand Voltage

Pasi Tamminen, Toni Viheriäkoski
Purpose

- CDM withstand information has to be adapted to practical protection actions in electronics industry
- Component assembly process differs from the CDM testing
- Simplified calculation methods should be used to assess CDM risks of different device packages in a placement process
Background and Motivation

- Dynamic ESD parameters are difficult to measure in a running assembly process.
- Electrostatic parameters can be measured from the process without long lasting interruptions.
- Electrostatic measurements and CDM withstand information together can be used to estimate CDM risks in an assembly process.
Outline

- Charged objects or components
  - In theory
  - In the CDM testing environment
  - In the component assembly environment
- Simplified calculation method
- Simulations for CDM testing and assembly
- Measured values for CDM testing and assembly
- Conclusions and discussion
Moving a Charged Object

- An object with a static charge $Q$ approaches a ground plane

- Two objects with static charges approaches each other
Calculation Method, CDM Testing

- CDM testing environment is simulated by calculating the changing capacitance between the DUT and grounding element of CDM tester with a fixed capacitance between the DUT and induction plate.
Calculations, CDM Testing

\[ V_B = \frac{C_G \cdot V_A}{C_G + C_{\text{Body}} + C_{\text{Pins}} + C_{\text{Pogo}}} \]
Calculation Method, Assembly

- Placement environment is simulated by calculating the size of the DUT and distances between the DUT and PWB
Calculations, Assembly

\[ C_{ESDS} = C_1 + \left( \frac{C_3 \cdot C_2}{C_3 + C_2} \right) \]

\[ C_{PWB} = C_2 + \left( \frac{C_1 \cdot C_3}{C_1 + C_3} \right) \]

\[ C_3 = \left( \frac{a_{\text{pins}} \cdot \varepsilon_0 \cdot \varepsilon_r}{d_{\text{pins}}} \right) + \left( \frac{(a_{\text{ESDS}} - a_{\text{pins}}) \cdot \varepsilon_0 \cdot \varepsilon_d}{(d_{\text{ESDS}} + d_{\text{pins}})} \right) \]

\[ V_{ESDS} = \frac{Q}{C_{ESDS}} \quad V_{PWB} = \frac{Q \cdot C_3}{C_{ESDS} \cdot (C_3 + C_{PWB})} \quad E = \frac{(V_{ESDS} - V_{PWB})}{d_{\text{PINS}}} \]
Components Used With The Study

- Land Grid Array (LGA), PLCC44 and DIL8 component packages were used in this study
Results of Simulated CDM Testing

[Graph showing the results of simulated CDM testing for different packages: LGA, PLCC44, and DIL8. The x-axis represents [mm] and the y-axis represents $[V]_1000$. The graph illustrates the comparison of voltage levels across different distances for each package type.]
Method of CDM Testing Measurement

- Potential of the component was measured with the high speed electrostatic voltage meter when the pogo pin was moving down to make the CDM discharge.
Results of CDM Testing Measurement

- Voltage drop of PLCC44 package during CDM discharge
- Voltage drop of DIL8 package during CDM discharge
LGA package was placed on a grounded PWB
Simulated Component Placement 2/6

- LGA package was placed on a floating PWB
Simulated Component Placement 3/6

- PLCC44 package was placed on a grounded PWB
Simulated Component Placement 4/6

- PLCC44 package was placed on a floating PWB
Simulated Component Placement 5/6

- DIL8 package was placed on a grounded PWB
Simulated Component Placement 6/6

- DIL8 package was placed on a floating PWB
Potential of the component was measured with the high speed voltage meter when the ground plate was moving down to make the CDM discharge.
Measured Placement Environment

- Measured potential of the LGA component when it moves to the 0.2mm distance from the PWB and is lifted away
Conclusions

- CDM type of ESD risks can be estimated by calculating initial CDM potentials before discharge
- Potential of the DUT will drop before discharge in the CDM testing environment
- Potential drop is significantly higher when component is placed on a surface of the PWB
- LGA type of component package has the safest shape for CDM sensitive components